# USB Keyboard Controller with 3-Port Hub MSE9751

## Introduction

The MSE9751 is a single chip keyboard controller with integrated 3-port Universal Serial Bus (USB) Hub. The MSE9751 USB Keyboard controller with Hub is highly integrated device requiring a minimum of external parts. The MSE9751 contains built-in transceivers, a 4X PLL clock generator with 12Mhz oscillator (requires external 12Mhz crystal), power-on reset, per-port over current detection, per-port power switching an on-board 3.3v regulator and internal key scan pullup resistors.

The USB portion of MSE9751 is implemented all in hardware and is fully compliant with *The Device Class Definition for Human Device Interface Device, Version 1.0*. Because the USB logic in the chip is implemented in hardware, the firmware programmer needs to write a very little code for USB functionality in the firmware.

The 8051 core in the chip shares the same instruction set as the standard 8051 microcontroller and provides the same internal registers and I/O interface, 4K mask ROM, multiple timers, 128 byte RAM and an additional watch dog timer. The four internal I/O ports are mapped to pre-assigned 18 scan-out pins and 10 scan-in pins. MSE9751 is the only USB keyboard controller in the industry that supports 18x10 scan matrix. MSE9751 provides five extra LED pins in addition to the standard three LED pins - Num Lock, Caps Lock and Scroll Lock. MSE9751 is again the only low-cost USB keyboard controller with integrated Hub that provides up to eight LED pins in total.

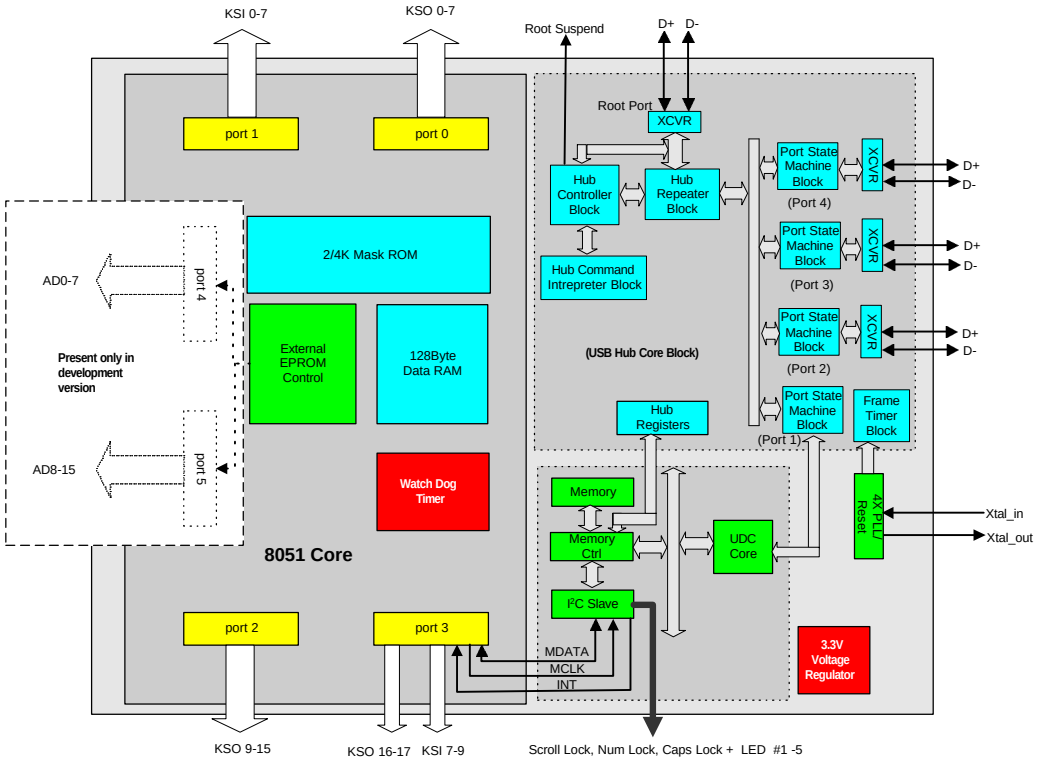
One major advantage of the MSE9751 is the fact that the USB descriptors which includes the standard descriptors and class-specific descriptors are not hard-coded in the chip. All descriptors are stored in the 8051 side and the 8051 gives descriptor contents to the USB logic when requested. This feature enables the firmware programmer to have a complete control over the makeup of the contents of all descriptors while developing a firmware. This flexibility is specially useful during the development of a report descriptor since finalizing a report descriptor usually requires an iterative process.

## MSE9751 Features

- Compliant with USB Protocol Revision 1.0
- Firmware required only for keyboard control
- 8051 Core with 4K Mask ROM and 128 byte RAM
- Three downstream ports
- Supports 18 scan-out lines, 10 scan-in lines
- Up to 8 Direct Drive LED's
- No external resistors required for key scan lines
- Full speed USB HID device
- Power management by supporting USB suspend/resume control
- Support for both low and full speed devices on the downstream ports
- Clock and data recovery from USB
- Bitstripping and Bitstuffing functions when the packets are addressed to the Hub
- CRC5 checking, CRC16 generation and checking for the packets addressed to the Hub
- Maintenance of the data toggle bits for the supported endpoints
- Output pin per port for port power switching mode and input pin per port for over-current detection
- Built-in transceivers for upstream and downstream ports

- Built-in voltage regulator
- Built-in 4X PLL clock generator
- Available in 64-pin PQFP package

## MSE9751 Block Diagram




## Pin Information

The following table shows pin descriptions for both 80-pin and 64-pin packages. The 80-pin package has 16 additional pins for accessing an external EPROM. The 80-pin package is the development version that allows the programmer to develop firmware using an in-circuit emulator. The pins whose numbers are in parenthesis are for the production version which contains the firmware in the internal ROM.

| Pin No. | | Pin Name | I/O Type | Description |
|---|---|---|---|---|
| **1** | (1) | PVDD | POWER | Analog Power for PLL ONLY. |
| **2** | (2) | XOUT | OUT | Oscillator Output. |
| **3** | (3) | XIN | IN | Oscillator Input. |
| **4** | (4) | AGND | POWER | Analog Ground for PLL ONLY.<br>Analog Ground for Analog Blocks except PLL. |
| **5** | (5) | AVDD | POWER | 5V Analog Power. |
| **6** | | AD_0 | IN/OUT | EPROM Address[0]/Data[0]. |
| **7** | (6) | TEST1n | IN | For Test. |
| **8** | | AD_1 | IN/OUT | EPROM Address[1]/Data[1]. |
| **9** | (7) | DP_OCn | IN | Over-current Indication Signal. |

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| **10** (8) | DP1_DP | IN/OUT | D+ for Downstream Port1. |
| **11** (9) | DP1_DM | IN/OUT | D- for Downstream Port1. |
| **12** | AD_2 | IN/OUT | EPROM Address[2]/Data[2]. |
| **13** (10) | DP2_DP | IN/OUT | D+ for Downstream Port2. |
| **14** (11) | DP2_DM | IN/OUT | D- for Downstream Port2. |
| **15** | AD_3 | IN/OUT | EPROM Address[3]/Data[3]. |
| **16** (12) | DP3_DP | IN/OUT | D+ for Downstream Port3. |
| **17** (13) | DP3_DM | IN/OUT | D- for Downstream Port4. |
| **18** (14) | RP_DP | IN/OUT | D+ for Upstream Port. |
| **19** (15) | RP_DM | IN/OUT | D- for Upstream Port. |
| **20** (16) | VDD1 | POWER | 5V Power for Digital Core.<br>5V Power for I/O PAD. |
| **21** (17) | DP_PWRONn | OUT | Power Control Signal for Downstream Ports. |
| **22** (18) | KSO_0 | IN/OUT | Key Scan Out_0. 200K Pull-down. *P0[0]* |
| **23** (19) | KSO_1 | IN/OUT | Key Scan Out_1. 200K Pull-down. *P0[1]* |
| **24** | AD_4 | IN/OUT | EPROM Address[4]/Data[4]. |
| **25** (20) | KSO_2 | IN/OUT | Key Scan Out_2. 200K Pull-down. *P0[2]* |
| **26** (21) | KSO_3 | IN/OUT | Key Scan Out_3. 200K Pull-down. *P0[3]* |
| **27** (22) | GND1 | POWER | Ground for I/O PAD.<br>Ground for Digital Core. |
| **28** | AD_5 | IN/OUT | EPROM Address[5]/Data[5]. |
| **29** (23) | KSO_4 | IN/OUT | Key Scan Out_4. 200K Pull-down. *P0[4]* |
| **30** (24) | KSO_5 | IN/OUT | Key Scan Out_5. 200K Pull-down. *P0[5]* |
| **31** (25) | VDD2 | POWER | Power for I/O PAD.<br>Power for Digital Core. |
| **32** (26) | KSO_6 | IN/OUT | Key Scan Out_6. 200K Pull-down. *P0[6]* |
| **33** (27) | KSO_7 | IN/OUT | Key Scan Out_7. 200K Pull-down. *P0[7]* |
| **34** | AD_6 | IN/OUT | EPROM Address[6]/Data[6]. |
| **35** (28) | KSO_8 | IN/OUT | Key Scan Out_8. 200K Pull-down. *P2[0]* |
| **36** (29) | KSO_9 | IN/OUT | Key Scan Out_9. 200K Pull-down. *P2[1]* |
| **37** (30) | KSO_10 | IN/OUT | Key Scan Out_10. 200K Pull-down. *P2[2]* |
| **38** | AD_7 | IN/OUT | EPROM Address[7]/Data[7]. |
| **39** (31) | KSO_11 | IN/OUT | Key Scan Out_11. 200K Pull-down. *P2[3]* |
| **40** (32) | KSO_12 | IN/OUT | Key Scan Out_12. 200K Pull-down. *P2[4]* |
| **41** (33) | KSO_13 | IN/OUT | Key Scan Out_13. 200K Pull-down. *P2[5]* |
| **42** (34) | KSO_14 | IN/OUT | Key Scan Out_14. 200K Pull-down. *P2[6]* |

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| **43** | AD_8 | IN/OUT | EPROM Address[8]/Data[8]. |
| **44** (35) | KSO_15 | IN/OUT | Key Scan Out_15. 200K Pull-down. *P2[7]* |
| **45** (36) | KSO_16 | IN/OUT | Key Scan Out_16. 200K Pull-down. *P3[6]* |
| **46** (37) | KSO_17 | IN/OUT | Key Scan Out_17. 200K Pull-down. *P3[7]* |
| **47** | AD_9 | IN/OUT | EPROM Address[9]/Data[9]. |
| **48** (38) | KSI_0 | IN/OUT | Key Scan In_0. 8K Pull-up. *P1[0]* |
| **49** (39) | KSI_1 | IN/OUT | Key Scan In_1. 8K Pull-up. *P1[1]* |
| **50** (40) | KSI_2 | IN/OUT | Key Scan In_2. 8K Pull-up. *P1[2]* |
| **51** (41) | KSI_3 | IN/OUT | Key Scan In_3. 8K Pull-up. *P1[3]* |
| **52** | AD_10 | IN/OUT | EPROM Address[10]/Data[10]. |
| **53** (42) | KSI_4 | IN/OUT | Key Scan In_4. 8K Pull-up. *P1[4]* |
| **54** (43) | KSI_5 | IN/OUT | Key Scan In_5. 8K Pull-up. *P1[5]* |
| **55** (44) | KSI_6 | IN/OUT | Key Scan In_6. 8K Pull-up. *P1[6]* |
| **56** (45) | KSI_7 | IN/OUT | Key Scan In_7. 8K Pull-up. *P1[7]* |
| **57** | AD_11 | IN/OUT | EPROM Address[11]/Data[11]. |
| **58** (46) | KSI_8 | IN/OUT | Key Scan In_8. 8K Pull-up. *P3[4]* |
| **59** (47) | KSI_9 | IN/OUT | Key Scan In_9. 8K Pull-up. *P3[5]* |
| **60** (48) | ALE | IN/OUT | Address Latch Enable Signal for M80C51. |
| **61** (49) | PSENn | IN/OUT | Program Strobe Enable Signal for M80C51. |
| **62** (50) | EAn | IN | External Access Enable Signal.<br>"H" : Internal ROM. "L" : External ROM. |
| **63** (51) | GND2 | POWER | Ground for I/O PAD. |
| **64** | AD_12 | IN/OUT | EPROM Address[12]/Data[12]. |
| **65** (52) | CAPSLn | OUT | Caps Lock LED. |
| **66** (53) | SCROLn | OUT | Scroll Lock LED.<br>When TEST1n is low, this pin will be used for PLL output. |
| **67** (54) | NUMLn | OUT | Num Lock LED.<br>When TEST1n is low, this pin will be used for TX_SDA output of the USB. |
| **68** | AD_13 | IN/OUT | EPROM Address[13]/Data[13]. |
| **69** (55) | GND3 | POWER | Ground for I/O PAD.<br>Ground for Digital Core. |
| **70** (56) | LED1n | IN/OUT | LED1.<br>When TEST1n is low, this pin will be used for p3[2] input to the M80C51. |
| **71** (57) | LED2n | IN/OUT | LED2. |

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| | | | When TEST1n is low, this pin will be used for SCL input to the USB. |
| **72** (58) | LED3n | IN/OUT | LED3.<br>When TEST1n is low, this pin will be used for SDA input to the USB. |
| **73** | AD_14 | IN/OUT | EPROM Address[14]/Data[14]. |
| **74** (59) | LED4n | IN/OUT | LED4.<br>When TEST1n is low, this pin will be used for MC_intr (*p3[3]* ) input to the M80C51 |
| **75** (60) | LED5n | OUT | LED5.<br>When TEST1n is low or TEST2 is high, this pin will be used for MC_intr output of the USB. |
| **76** (61) | TEST2 | IN | M80C51 Select.<br>"H" : Use the Internal M80C51.<br>"L" : Use the External M80C51. |
| **77** | AD_15 | IN/OUT | EPROM Address[15]/Data[15]. |
| **78** (62) | SDA | IN/OUT | Serial Data for the external M80C51. |
| **79** (63) | SCL | IN | Serial Clock for the external M80C51. |
| **80** (64) | V3P3 | OUT | 3.3V Voltage Regulator Output. |

*note: Pin numbers in () are for 64-pin QPFP package